ICH8500/A
Ultra Low Input-Bias Operational Amplifier

GENERAL DESCRIPTION

The ICH8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20kΩ potentiometer. The input bias current for the inverting and noninverting inputs is 0.1pA maximum for the ICH8500, and 0.01pA maximum for the ICH8500A.

Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential. This is the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

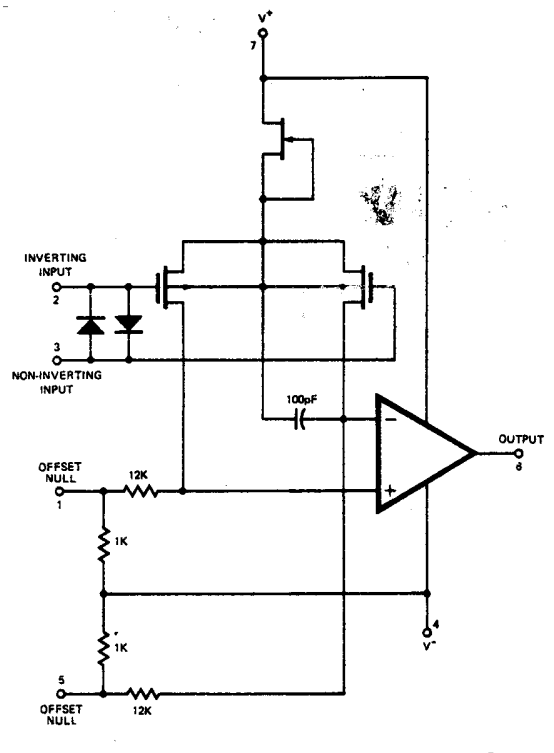

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Figure 1: Functional Diagram

FEATURES

- **Input Diode Protection**
- **Input Bias Current Less Than 0.01pA (8500A)**
- **No Frequency Compensation Required**
- **Offset Voltage Null Capability**
- **Short Circuit Protection**
- **Low Power Consumption**

APPLICATIONS

- **Femto Ammeter**
- **Electrometers**
- **Long Time Integrators**
- **Flame Detectors**
- **pH Meters**
- **Proximity Detector**
- **Sample and Hold Circuits**

ORDERING INFORMATION

ICH 8500A TV

PACKAGE
TV = TO-99 Metal Can

DEVICE TYPE

INTERSIL HYBRID CIRCUIT

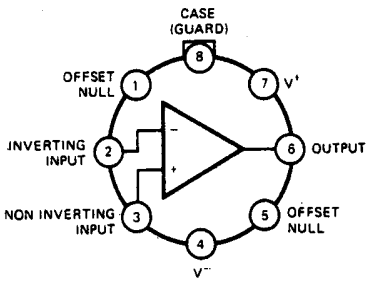

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Figure 2: Pin Configuration (Outline dwg TV)

NOTE: All typical values have been characterized but are not tested.

ICH8500/A

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (1) 500mW
Differential Voltage ..... ±0.5V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −25°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Output Short Circuit Duration ..... Indefinite

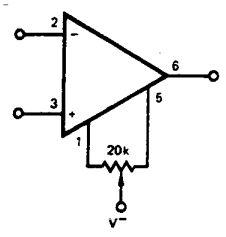
Note: 1. Rating applies for ambient temperature to +70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPPLY} = ±15V)

Symbol	Characteristics	Test Conditions	ICH8500			ICH8500A			Units
			Min	Typ	Max	Min	Typ	Max	
I_{BIAS}	Input Bias Current (Inverting and Non-Inverting)	Case at same potential as inputs			±0.1			±0.01	pA
V_{OS}	Input Offset Voltage				±75			±50	mV
	Offset Voltage Adjustment Range	20kΩ Potentiometer		±50			±50		mV
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage Over Temperature	+25 to +85°C −25 to +25°C		±200			±100		mV
$\Delta V_{OS}/\Delta t$	Long Term Input Offset Voltage Stability	At 25°C		±3.0			±3.0		mV
CMRR	Common Mode Rejection Ratio	±5 volts common mode voltage		75			75		dB
ΔV_O	Output Voltage Swing	$R_L \geq 10k\Omega$	±11			±11			V
CMVR	Common Mode Voltage Range		±10			±10			V
A_{VOL}	Large Signal Voltage Gain		20,000	10^5		20,000	10^5		—
C_{fb}	Feedback Capacitance	Case guarded		0.1			0.1		pF
SR	Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μs
C_{IN}	Input Capacitance	Case guarded		0.7			0.7		pF
C_{IN}	Input Capacitance	Case grounded		1.5			1.5		pF

VOLTAGE OFFSET NULL CIRCUIT



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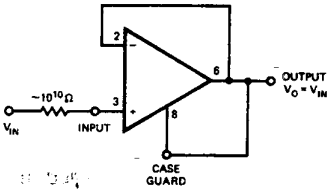
VOLTAGE FOLLOWER



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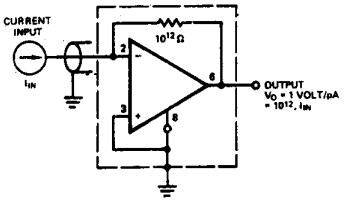
LOW LEVEL CURRENT MEASURING CIRCUIT



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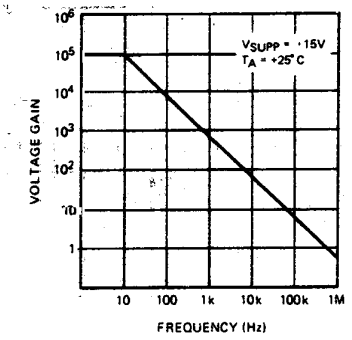
NOTE: Adjust input offset voltage to 0V ± 10μV before measuring leakage.

Figure 3: Circuit Notes

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



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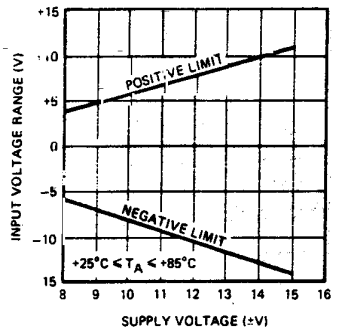
INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



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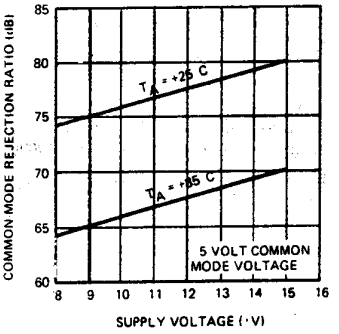
COMMON MODE REJECTION RATIO vs. SUPPLY VOLTAGE



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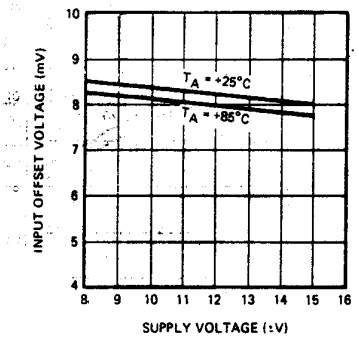
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



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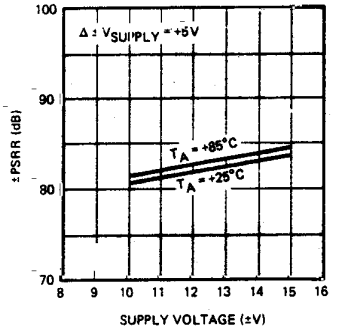
±POWER SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



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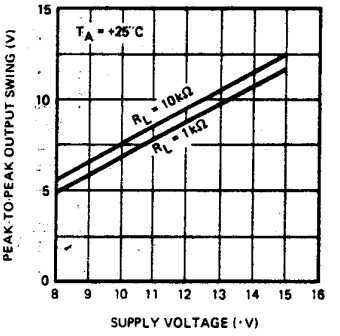
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



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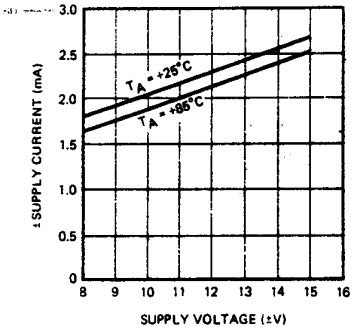
±QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



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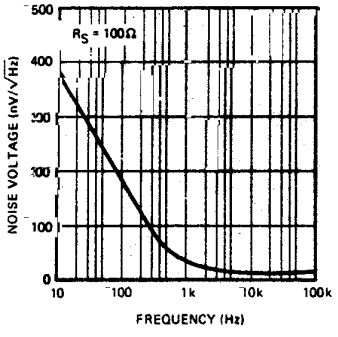
INPUT REFERRED NOISE VOLTAGE



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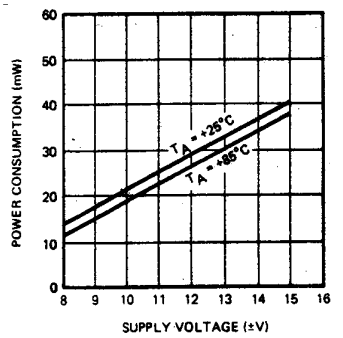
POWER CONSUMPTION vs. SUPPLY VOLTAGE



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NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 4) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case the potential of the input is at virtual ground, or 0V. Therefore, the case of the device is grounded to intercept any stray leakage currents that may otherwise exist between the ±15V input terminals and the inverting input summing junctions. Feedback capacitance* should be kept to a minimum in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{fb} times the feedback resistor R_{fb}. For instance, the time constant of the circuit in Figure 4 is 1 sec if $C_{fb} = 1pF$. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{fb} of less than 0.2 to 0.3pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 5.

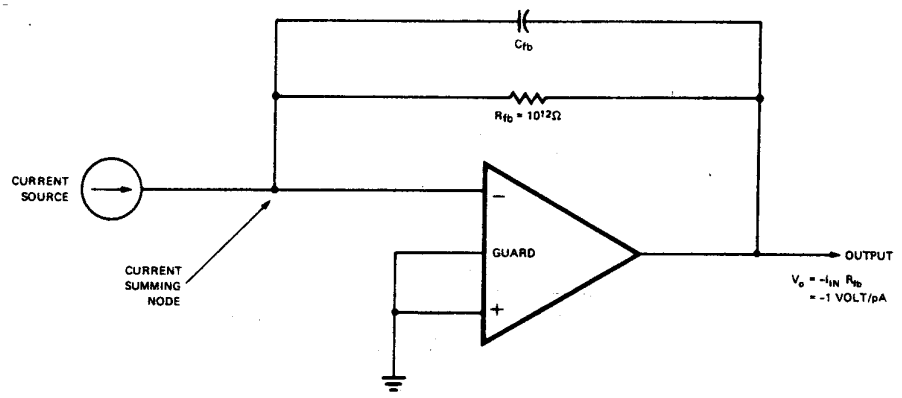

Figure 4: Basic Pico Ammeter Circuit

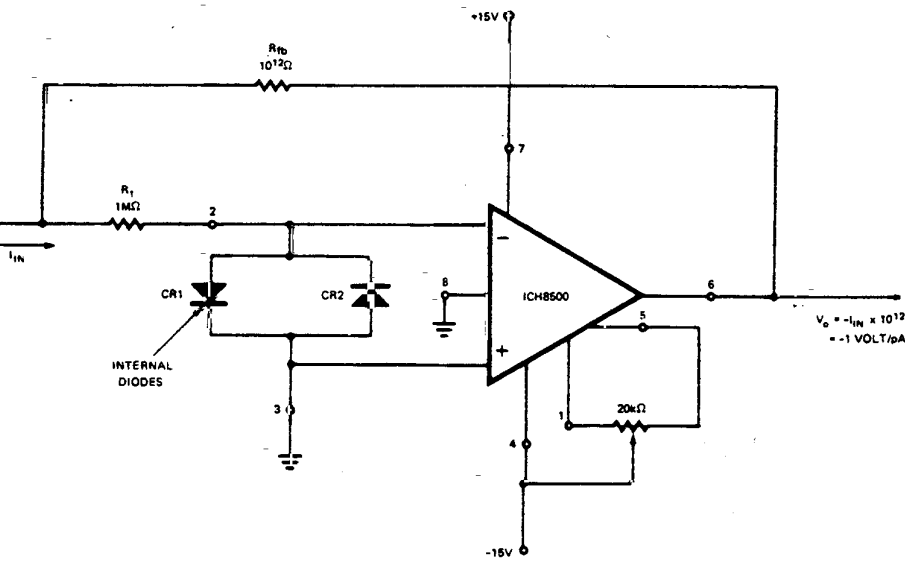

Figure 5: Pico Ammeter Circuit

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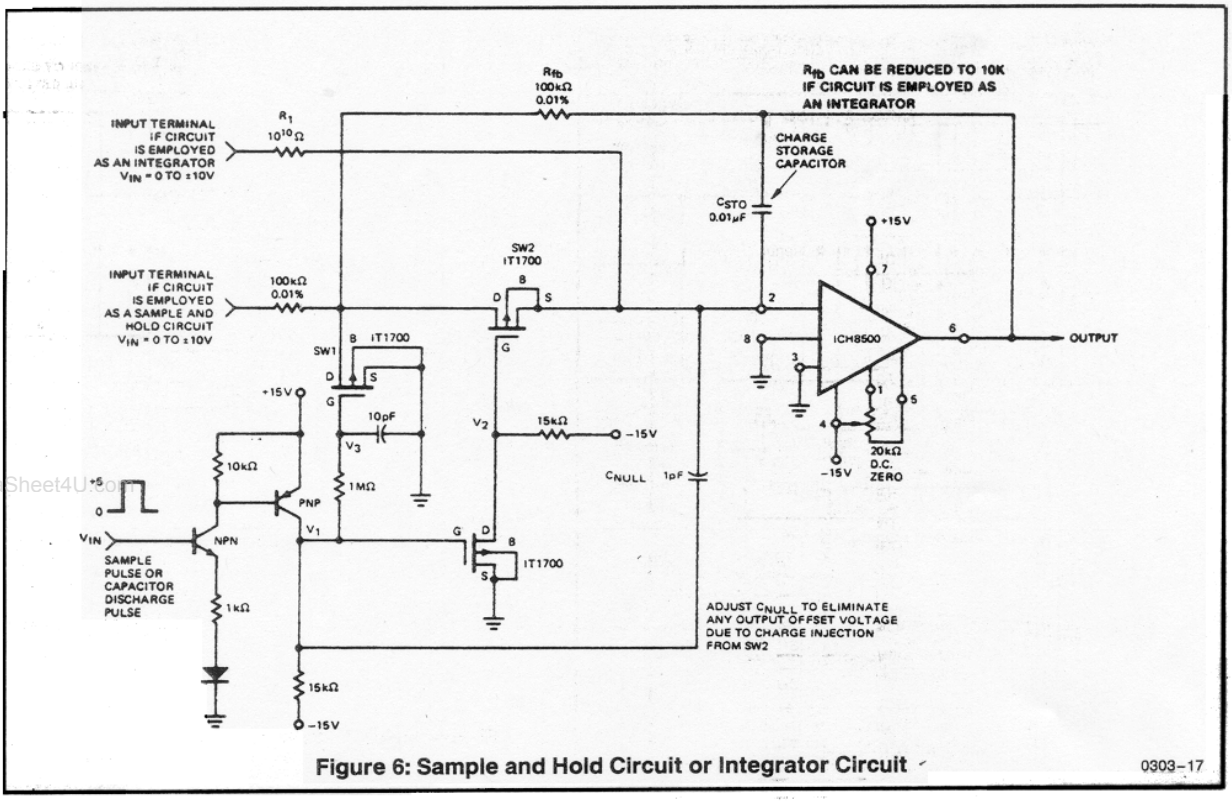

Figure 6: Sample and Hold Circuit or Integrator Circuit 0303-17

The internal diodes CR1 and CR2 together with external resistor R1 protect the input stage of the amplifier from voltage transients. The two diodes contribute no error currents, since under normal operating conditions there is no voltage across them.

*Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

Sample and Hold Circuit

The basic principle of this circuit (Figure 6) is to rapidly charge a capacitor C_{STO} to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_{STO}. Since C_{STO} is in the negative feedback loop of the operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_{STO} should remain constant, causing the output of the amplifier to remain constant as well. However, the voltage across C_{STO} will decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_{STO}, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (<0.01pA). Note that the voltages on the source, drain and gate of switch SW2 are zero or near zero when the circuit is in the hold mode. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a low drift sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the 0.01μF storage capacitor is then 10mV/sec. In contrast, if an operational amplifier which exhibited an input bias current of 1nA were employed, the rate of change of the voltage across C_{STO} would be 0.1V/sec. An error build up such as this could not be tolerated in most applications.

Waveforms illustrating the operation of the sample and hold circuit are shown in Figure 7.

The Gated Integrator

The circuit in Figure 6 can double as an integrator. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and C_{STO}. Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (Up to 10^{12} ohms) can be employed. This permits the use of small values of integrating capacitor (C_{STO}) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 8.

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ICH8500/A

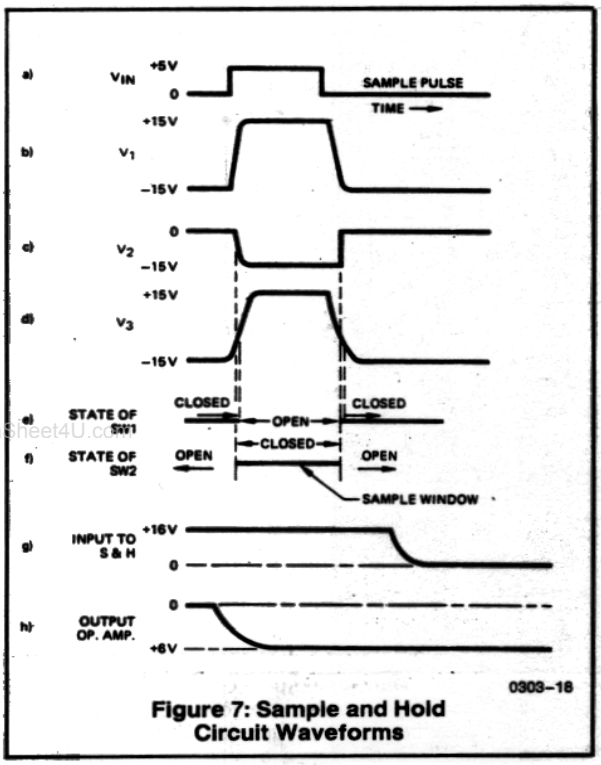

Figure 7: Sample and Hold Circuit Waveforms

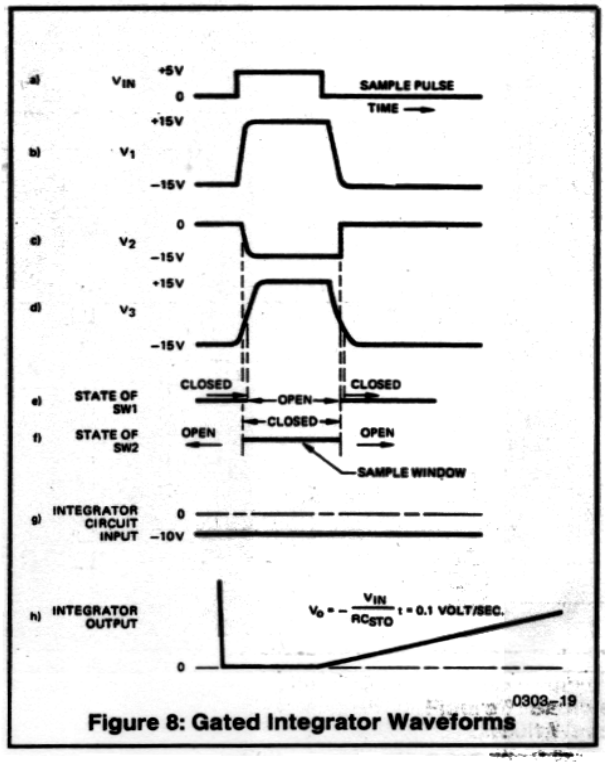

Figure 8: Gated Integrator Waveforms

NOTE: All typical values have been characterized but are not tested.